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APPLICATION FOR LETTERS PATENT

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WAFER-LEVEL CHIP SCALE PACKAGE AND METHOD FOR FABRICATING AND USING THE SAME

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[001] REFERENCE TO RELATED APPLICATIONS

[002] This application is a continuation-in-part of U.S. Patent Application Number 10/295,281, the entire disclosure of which is incorporated herein by reference.

[003] FIELD OF THE INVENTION

[004] The invention generally relates to methods for fabricating integrated circuits (ICs) and semiconductor devices and the resulting structures. Specifically, the invention relates to a semiconductor package and a method for fabricating and using the same. More particularly, the invention relates to a wafer level chip scale package and a method for fabricating and using the same.

[005] BACKGROUND OF THE INVENTION

[006] Recent advancements in the electronics industry, especially with personal computers (PC), mobile phones, and personal data assistants (PDA), have triggered a need for light, compact, and multi-functional power systems that can process large amounts of data quickly. These advancements have also triggered a reduction in the size of semiconductor chips and the packaging used for these chips. One type of

packaging that has recently been used is wafer-level chip size packaging (WLCSP). See, for example, U.S. Patent Nos. 6187615 and 6287893, the disclosures of which are incorporated herein by reference.

[007] In general, to fabricate WLCSP, a wafer is processed and then packaged by a photolithography process and a sputtering process. This method is easier than general packaging processes that use die bonding, wire bonding, and molding. Processes for WLCSP also have other advantages when compared to general packaging processes. First, it is possible to make solder bumps for all chips formed on a wafer at a time. Second, a wafer-level test on the operation of each semiconductor chip is possible during WLSCP processes. For these—and other reasons—WLCSP can be fabricated at a lower cost than general packaging.

[008] Figures 1-3 illustrate several known wafer-level chip scale packages. As shown in FIG. 1, chip pads 40 are formed of a metal such as aluminum on a silicon substrate 5. A passivation layer 10 is formed to expose a portion of each of the chip pads 40 on the silicon substrate 5 while protecting the remainder of the silicon substrate 5. A first insulating layer 15 is formed over the passivation layer 10 and then a re-distribution line (RDL) pattern 20 (which re-distributes electrical signals from the bond pad 40 to solder bump 35) is formed over portions of the first insulating layer 15 and the exposed chip pads 40. A second insulating layer 25 is formed on portions of the RDL pattern 20 while leaving portions of the RDL pattern 20 exposed. Under bump metals (UBM) 30 are formed between solder bumps 35 and the exposed portions

of the RDL pattern 20. The RDL pattern 20 contains inclined portions on the first insulating layer 15 near the chip pads 40. In these areas, short circuits can occur and the pattern 20 can crack and deform in these areas due to stresses.

[009] As depicted in FIG. 2, package 50 contains an RDL pattern 54 that adheres to a solder connection 52 in a cylindrical band. Such a configuration has several disadvantages. First, the contact area between the RDL pattern 54 and the solder connection 52 is minimal, thereby deteriorating the electrical characteristics between them. Second, short circuits may occur due to the stresses in the contact surface between the RDL pattern 54 and the solder connection 52. Third, the solder connection 52—which is connected with a solder bump 58 formed on a chip pad 56—is exposed to the outside of the package 50, i.e., to air. Thus, there is a higher possibility that moisture penetrates into the solder connection 52 and decreases the reliability of the solder connection 52. Fourth, the package 50 is completed only by carrying out many processing steps and, therefore, manufacturing costs are high.

[0010] As shown in FIG. 3, package 60 contains a RDL pattern 76 that is electrically connected with a chip pad 72 via a connection bump 74. The RDL pattern 76 is, however, inclined on the connection bump 74, causing cracks therein due to stresses as described above. As well, the connection bump 74 is made by a plating process and is formed of aluminum, copper, silver, or an alloy thereof. Accordingly, the package 60 is not easy to manufacture.

[0011] Other problems exist with conventional WLSCP. Often, such packaging uses UMB (i.e., layer 30 in FIG. 1) and two insulating layers (i.e., layers 15 and 25 in FIG.1) that are made of polymeric materials such as polyimide and benzocyclobutene (BSB). Such structures are complicated to manufacture. As well, the coefficient of thermal expansion (CTE) between the various layers can induce thermal stresses into the ICs and damage the ICs during high temperature curing of these polymeric materials.

[0012] SUMMARY OF THE INVENTION

[0013] The invention provides a packaged semiconductor device (a wafer-level chip scale package) containing no UBM between a chip pad and an RDL pattern. As well, the device contains only a single non-polymeric insulation layer between the RDL pattern and the solder bump. The single non-polymeric insulation layer does not need high temperature curing processes and so does not induce thermal stresses into the device. As well, manufacturing costs are diminished by eliminating the UBM between the chip pad and the RDL pattern.

[0014] BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figures 1-17 are views of one aspect of the devices and methods of making the devices according to the invention, in which:

[0016] Figure 1 is a cross-sectional view of a conventional wafer-level chip scale page;

[0017] Figure 2 is a cross-sectional view of another conventional wafer-level chip scale package;

[0018] Figure 3 is a cross-sectional view of another conventional wafer-level chip scale package;

[0019] Figure 4 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0020] Figure 5 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0021] Figure 6 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0022] Figure 7 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0023] Figure 8 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0024] Figure 9 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0025] Figure 10 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0026] Figure 11 is a cross-sectional view of a wafer-level chip scale package according to another aspect of the invention;

[0027] Figures 12-15 illustrate stages in a method of fabricating a wafer-level chip scale package in one aspect of the invention;

[0028] Figure 16 depicts another stage in a method of fabricating a wafer-level chip scale package in one aspect of the invention; and

[0029] Figure 17 depicts a process for making a wafer-level chip scale package in another aspect of the invention.

[0030] Figures 1-17 presented in conjunction with this description are views of only particular—rather than complete—portions of the devices and methods of making the devices according to the invention. Together with the following description, the Figures demonstrate and explain the principles of the invention. In the Figures, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. The same reference numerals in different drawings represent the same element, and thus their descriptions will be omitted.

[0031] DETAILED DESCRIPTION OF THE INVENTION

[0032] The invention will now be described more fully with reference to the accompanying drawings, in which one aspect of the invention is shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the aspects set forth herein. Rather, these aspects are

provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art. Although the invention is described with respect to IC chips, the invention could be used for other devices where packaging is needed, i.e., silicon MEMS devices.

[0033] FIGS. 4 through 10 illustrate one aspect of the invention for fabricating a wafer-level chip scale package containing a re-distributed line (RDL) pattern that is not inclined between the bottom of a solder bump and the top surface of a chip pad. Referring to FIG. 4, a substrate 100 is prepared on which a passivation layer 110 and a chip pad 115 are formed. The substrate 100 can be any known semiconductor substrate known in the art, including "compound" semiconductors and single crystal silicon. The passivation layer 110 can be made of any dielectric material known in the art, such as silicon nitride, silicon oxide, or SOG.

[0034] Then, the chip pad 115 is formed on the upper surface of substrate 100. First, a portion of passivation layer in this area is removed by a conventional masking and etching process. Then, the metal for the chip pad 115 is blanket deposited and the portions of the metal layer not needed for the bond pad are removed by etching or planarization. The chip pad 115 can be made of conductive material, such as metals and metal alloys. In one aspect of the invention, the chip pad comprises aluminum.

[0035] A wire 120 is next attached to the chip pad 115 using a capillary 130. As shown in FIG. 5, the bottom of the wire 120 is bonded to the chip pad 115. Then a coining process is performed to press the wire 120 under a predetermined pressure,

thereby forming a coined stud bump 125. By using the capillary 130, the coined stud bump 125 can be formed with a simple structure and with a simple manufacturing process.

[0036] As depicted in FIG. 6, a first insulating layer 135 is then deposited to cover the coined stud bump 125 and passivation layer 110. In this aspect of the invention, the first insulating layer 135 is formed of a dielectric polymer material such as BCB, polyimide (PI), and EMC. As illustrated in FIG. 7, the first insulating layer 135 and the coined stud bump 125 are planarized using conventional processing. In the planarization process, a stud bump 125' and a first insulating layer 135' are formed. In one aspect of the invention, a chemical mechanical polishing (CMP) process is used to planarize the first insulating layer 135 and the stud bump 125.

[0037] As shown in FIG. 8, a re-distributed line (RDL) pattern 140 is formed on the stud bump 125' and the first insulating layer 135'. The RDL pattern 140 electrically connects the stud bump 125' and the solder bump that is formed during subsequent processing (as described below). The RDL pattern is formed by blanket depositing a metal layer and then removing—typically by masking and etching—the portions of the metal layer not needed for the DRL pattern 140. The RDL pattern 140 can contain any electrically conductive material, such as metals and metal alloys. Examples of such metal and metal alloys include Cu, Al, Cr, NiV, and Ti. In one aspect of the invention, the RDL comprises a composite layer of Cu, Al, Cr, and Cu, or a material selected from NiV and Ti. In conventional wafer-level chip scale package as shown in FIG. 1, the

RDL pattern 20 was formed of Al, NiV, Cu, NiV, and Cu that are sequentially deposited on the chip pad 40. Such a configuration has poor adhesive characteristics and reliability, is not easy to fabricate, and has high manufacturing costs.

[0038] As depicted in FIG. 9, a second insulating layer 150 is then formed to cover the RDL pattern 140 and the first insulating layer 135'. A portion of the second insulating layer 150 is removed—typically by masking and etching—to expose a portion of the RDL pattern 140 to which a solder bump is later attached. As shown in FIG. 10, a solder bump 160 is then attached to the exposed portion of the RDL pattern 140 as known in the art. The stud bump comprises any conductive material such as metal and metal alloys. In one aspect of the invention, the stud bump comprises gold (Au) or copper (Cu).

[0039] The wafer-level chip scale package 1000 is illustrated in FIG. 10. The silicon substrate 100 contains an IC (not shown) and chip pad 115 which extends into the passivation layer 110 and is encircled by the passivation layer 110. Electrical signals from the IC contained in substrate 100 are transmitted through chip pad 115, through RDL pattern 140, to solder bump 160, and then to the outside of the packaged semiconductor device (i.e., to a circuit board).

[0040] In the device of FIG. 10, the first insulating layer 135' encircles and covers the stud bump 125'. Since the top surface of the first insulating layer 135' and stud bump 125' are coplanar in this aspect of the invention, the RDL pattern 140 may be formed as

a substantially planar layer without an inclined portion. Therefore, cracks in the RDL pattern 140 due to stresses are prevented.

[0041] The RDL pattern 140 shown in FIG. 10 is illustrated as on only a portion of the upper surface of the stud bump 125'. In another aspect of the invention, the RDL pattern can be formed to cover the entire stud bump 125', thus enhancing the electrical characteristics and reliability of the wafer-level chip scale package 1000.

[0042] The RDL pattern 20 of FIG. 1 contains an inclined portion in the conventional wafer-level chip scale package. Accordingly, it is extremely difficult to form a thick first insulating layer 15 in FIG. 1. In this aspect of the invention, however, the first insulating layer 135' in FIG. 10 is formed as a thick layer.

[0043] FIG. 11 illustrates another aspect of the invention where a wafer-level chip scale package has a two-layer RDL pattern. A wafer-level chip scale package 2000 contains: a substrate 100; a passivation layer 110; chip pads 115; stud bumps 125' that are formed on chip pads 115 and are encircled by a first insulating layer 135'; intermediate RDL pattern 210 that connects the stud bumps 125' and intermediate stud bumps 220; an intermediate insulating layer 230 that insulates the intermediate RDL pattern 210; RDL pattern 140 that connects the intermediate stud bumps 220 and solder bumps 160; a second insulating layer 150 that insulates the RDL patterns 140; and solder bumps 160 that are attached to a portion of each of the RDL pattern 140.

[0044] Components not described in FIG. 11 are the same as those components explained with reference to FIG. 10. The same reference numerals in FIGS. 10 and 11

denote the same elements that have substantially the same functions and are formed of the same materials and in substantially the same manner. The structure, functions, materials, and effects of the intermediate stud bumps 220, the intermediate RDL pattern 210 and the intermediate insulating layer 230 are substantially the same as those of the stud bump 125, the RDL pattern 140, and the second insulating layer 150, respectively. The intermediate stud bumps 220 connect the intermediate RDL pattern 210 and the RDL pattern 140. Each intermediate RDL pattern 210 is formed at the bottom of each intermediate stud bump 220. The intermediate insulating layer 230 exposes a portion of the intermediate RDL pattern 210 so it can be connected with the intermediate stud bumps 220.

[0045] In another aspect of the invention, additional intermediate stud bumps, intermediate RDL patterns, and intermediate insulating layers may be formed to make a three (or more) layer RDL pattern rather than the two layer RDL pattern illustrated in FIG. 11.

[0046] In the aspects of the invention described above, it is possible to reduce or prevent an inclined portion of a RDL pattern in the art between a solder bump and a chip pad. Such a configuration suppresses cracks in the RDL pattern, even where an underlying insulating layer has a large thickness. Further, a stud bump can be easily and inexpensively formed using a capillary.

[0047] In another aspect of the invention, the wafer level chip scale package is manufactured in the manner depicted in Figures 12-17 so as to not contain a UBM

between the chip pad the RDL pattern and to contain a single non-polymeric insulating layer. In this aspect of the invention, and as depicted in Figure 17, the bond pads are first redistributed (as depicted in more detail in Figures 12-15). Then, the stud bumps are formed on the wafer (as depicted in more detail in FIG. 16). The solder balls are then attached to the stud bumps, either directly or by using solder paste, and the solder balls are re-flowed. The resulting packaged semiconductor device can then be mounted on a circuit board as known in the art.

[0048] In this aspect of the invention, and as illustrated in Figures 12-13, a substrate 300 (substantially similar to substrate 100) containing IC 305 is obtained. A passivation layer 310 (substantially similar to passivation layer 110) is then formed on substrate 300. A portion of the passivation layer is then removed and a chip pad 315 (substantially similar to chip pad 115) is formed in that exposed portion. The methods used for these processes are substantially similar to those described above.

[0049] Next, as depicted in FIG. 14, a re-distributed (RDL) pattern 340 is formed directly on the chip pad 315 and the passivation layer 310. The RDL pattern 340 electrically connects the chip pad 315 and the solder bump 365 that is formed during subsequent processing (as described below). The RDL pattern 340 is formed by blanket depositing a metal layer and then removing—typically by masking and etching—the portions of the metal layer not needed for the RDL pattern 340. The RDL pattern 340 can contain any electrically conductive material, such as metals and

metal alloys. Examples of such metal and metal alloys include Cu, Al, Cr, NiV, and Ti. In one aspect of the invention, the RDL pattern comprises Al.

[0050] Next, as shown in FIG. 15, an insulating layer 350 is formed to cover the RDL pattern 340. In this aspect of the invention, the material for the insulating layer is blanket deposited on the RDL pattern 340. A masking and etching process is then used to remove a portion of this insulating material in the area of region 375 (where stud bumps 365 will later be formed).

[0051] The material for the insulating layer 350 does not comprise a polymer material like BCB, PI, and EMC. As described above, such materials are often used in conventional WLCSP. To form such layers, however, the structure containing the material is subjected to a high temperature heating process. This heating is necessary to cure the polymer material. Unfortunately, such a high temperature heating process damages the structure underlying the polymeric material including the IC 305 in substrate 300.

[0052] In this aspect of the invention, the insulating layer 350 is not made of polymeric materials. Rather, the insulating layer 350 is made of dielectric non-polymeric materials. Examples of such non-polymeric dielectric materials include silicon nitride, silicon oxide, and silicon oxynitride. Such materials can be deposited by any known method in the art.

[0053] In this aspect of the invention, only a single layer is used as the redistribution layer. In the aspect of the invention shown in Figures 4-10, a UBM and a metal layer

are used to redistribute the electrical signal from the chip pad 115 to the stud bump 160. By using only a metal layer in this aspect of the invention, the cost of the manufacturing the UBM can be eliminated. Thus, this aspect of the invention uses only a single conductive layer as the RDL pattern in the WLSCP.

[0054] As depicted in FIG. 16, the stud bumps are then formed on the exposed portion of the RDL pattern 340 (in the area 375). The stud bumps 365A can be formed by electroplating the material for the stud bumps with a cladding as known in the art. In this aspect of the invention, the material for the study bumps is Cu and the cladding is a Ni/Au alloy.

[0055] Alternatively, the stud bumps 365B can be formed by a wire bonding process. In this aspect of the invention, a coated wire 380 is attached to the RDL pattern 340 using a capillary 385. As shown in FIG. 16, the bottom of the wire 380 is first bonded to the metal of the RDL pattern 340. Then a coining process is performed to press the wire 380 under a predetermined pressure to form a coined stud bump 365B. By using the capillary, the coined stud bump 365B can be formed with a simple structure and with a simple manufacturing process. In one aspect of the invention, the material for the wire comprises Cu and the coating comprises Pd.

[0056] Finally, as shown in FIG.17, the solder balls are then attached to the stud bumps, either directly or by using solder paste, and the solder balls are re-flowed. Both of these processes are performed using conventional processing that is known in the art.

[0057] Having described these aspects of the invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.